Please add the following claims 24-44:

24. (New) A phase lock loop comprising:

a detector adapted to receive an input data signal;

a timing reference signal generator coupled to said detector; and

a charge pump coupled to said detector, said charge pump comprising:

first and second current sources;

first and second parallel current paths coupled at first ends to said first current source and coupled at second ends to said second current source, said first and second current paths having respective first and second output nodes;

a filter coupled to said first output node;

a capacitor coupled to said second output node; and

a feedback means coupled at a first input to said filter, at a second input to said capacitor, and at an output to one of said first and second current sources, said feedback means adapted to balance currents in said first and second current sources to minimize DC offset and glitch energy at a charge pump output node.

25. (New) The phase lock loop of claim 24, wherein said charge pump is implemented using CMOS technology.

26. (New) The phase lock loop of claim 24, wherein said feedback means is coupled to one of said first and second current sources via an adjusting current source.

27. (New) The phase lock loop of claim 24, wherein said feedback means is coupled directly to said first current source.

28. (New) The phase lock loop of claim 24, wherein said feedback means is coupled directly to said second current source.

29. (New) The phase lock loop of claim 24, wherein an adjusting current source is coupled between said feedback means and said first current source.

30. (New) The phase lock loop of claim 24, wherein an adjusting current source is coupled between said feedback means and said second current source.

31. (New) The phase lock loop of claim 24, wherein said filter is an analog loop filter.

32. (New) The phase lock loop of claim 24, wherein said feedback means is a transconductance amplifier.

33. (New) The phase lock loop of claim 24, wherein said filter comprises:

a resistor;

a first capacitor coupled in series with said resistor; and

a second capacitor coupled in parallel with said series resistor and first capacitor;

wherein an input to said feedback means is coupled to a node between said resistor and said first capacitor.

34. (New) The phase lock loop of claim 24, wherein said capacitor is a dump capacitor.

35. (New) The phase lock loop of claim 24, wherein said first current path comprises:

a first switching device; and

a second switching device;

wherein said first output node is located between said first and second switching devices.

36. (New) The phase lock loop of claim 35, wherein said first and second switching devices are transistors.

37. (New) The phase lock loop of claim 24, wherein said second current path comprises:

a first switching device; and

a second switching device;

wherein said second output node is located between said first and second switching devices.

38. (New) The phase lock loop of claim 37, wherein said first and second switching devices are transistors.

39. (New) A method of controlling a charge pump, the method comprising the steps of:

detecting an input signal and a timing reference signal with a detector, said detector then outputting a pump-up and pump-down signal;

receiving said pump-up and said pump-down signal at a charge pump;

transmitting said pump-up and said pump-down signals through first and second parallel current paths that are coupled between first and second current sources in said charge pump;

outputting a first current path output signal from said first current path to a filter, said filter producing a filter output signal;

outputting a second current path output signal from said second current path to a capacitor;

receiving said filter output signal and said second current path output signal at inputs of a feedback means, said feedback means generating a feedback output signal; and

balancing currents in said first and second current sources using said feedback output signal to minimize D.C. offsets and glitch energy.

40. (New) The method of claim 39, further comprising the step of directly adjusting said first current source with said feedback output signal.

41. (New) The method of claim 39, further comprising the step of directly adjusting said second current source with said feedback output signal.

42. (New) The method of claim 39, further comprising the steps of:

receiving said feedback output signal at an adjusting current source; and

performing said balancing of said current in said first and second current sources via said feedback means and said adjusting current source.

43. (New) The method of claim 42, further comprising the step of coupling said adjusting current source directly to said first current source.

44. (New) The method of claim 42, further comprising the step of coupling said adjusting current source directly to said second current source.

45. (New) A method of controlling a charge pump having two parallel current paths formed of transistors, each current path coupled between a first current source and a second current source, said charge pump operating within a phase lock loop, the method comprising the steps of:

detecting a phase or frequency characteristic of an input signal to produce an output signal;

receiving said output signal at said charge pump and using said output signal to produce a charge pump control signal;

generating a characteristic current using one of said first current path and said second current path in response to said charge pump control signal; and

controlling a value of one of said first current source and said second current source to minimize D.C. offsets resulting from parasitic capacitances of said transistors.

***In the Abstract:***

Please replace the Abstract of the Disclosure with the new Abstract enclosed herewith on a separate page.